REMARKS/ARGUMENTS

Reconsideration and re-examination are hereby requested.

Claims 1 and 2 stand rejected under 35 U.S.C. 102(b) as being anticipated by Gaytan et al. (US 5,638,367).

As pointed out in claim 1, the system includes:

> a shifter for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets.

The Examiner appears to equate this with the word packing circuit 600 in FIG. 6a of Gaytan et al. The word packing circuit 600 of Gaytan et al. takes two 32 bit portions of a parallel 64 bit word (one 32 bit portion we will refer to herein as portion a 32 bit portion A being fed to latch 605 and the other 32 bit portion we will refer to herein as portion a 32 bit portion B being fed to latch 615). The word packer 600 converts the 64 bit word into a 32 bit word at the output of selector 625; portion A appearing first in tine and then portion B appearing subsequent to portion A in time. Therefore, the word packer 600 does not shift the bytes stored in the sampling register, such bytes being shifted as a function of ***the offset*** of the ***currently gathered one of the packets*** and the number of bytes in ***a prior gathered one of the packets.*** See Column 6, Line 61 of the Gaytan et al. patent where it speaks of the basis of the setting for the Selectors 610 and 615 of Fig. 6a as being: "the value of bit 2 of the starting address of valid data within an associated TX data buffer". In other words, the configuration of the Selectors is based on the offset (starting address) of the currently gathered packet with ***no component referenced which is related to the prior gathered packet.***

Claim 1 then points out that there is an accumulator register having W byte locations for storing ***the shifted bytes*** in response to a clock pulse.

The Examiner refers to element 660 as an accumulator register; however, since element 600 is not a shifter as claimed by the applicant, element 660 does not store ***the shifted bytes*** referred to in applicant's claim and thus element 600 is not the accumulator register referred to by the claim.

To put it in still another way, Applicant stores in sampling register 600, then FIRST SHIFTS in shifter 602 bytes as a ***function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets***, then sends the SHIFTED data to an accumulator 604 and staging register 606 with the SHIFTED data in the accumulator 604 being fed directly to one input of a multiplexer 608 and the SHIFTED data in the staging register 606 being fed to a second input of the multiplexer 608. Such an arrangement is not described in Gaytan et al. (US 5,638,367).

It is noted that this difference was pointed out to the Examiner in response to the first office action and is repeated here for convenience:

> It is respectfully submitted that a elements 610 and 615 of Gaytan et al. (US 5,638,367) DO NOT shift the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets (col. 6, lines 53-65) BUT RATHER selects different portions of the word. As stated in col. 6, lines 53-65:
>
> > As shown, the lower data word is transferred into (i) the latch element 605, (ii) a first port of the first input selector 610 and (iii) a first port of the input second selector 615 during a first transfer cycle. The upper data word is input into a second port of the second input selector 610. These first and second input selectors 610 and 615 are configured to be disabled to prevent an invalid word (32-bits) from being written into the read storage element 620 by setting Select1 equal to logic "1" and Select0 equal to the value of bit 2 of the starting address of valid data within an associated TX data buffer of the host memory. It is contemplated that the configuration of the Select0,1 lines can be deduced for all sizes of the system bus

(e.g., "00" for 32-bit system bus). (emphasis added)

Thus, it is respectfully submitted that a elements 610 and 615 of Gaytan et al. (US 5,638,367) DO NOT shift the bytes stored in the sampling register. It is noted that Gaytan et al. (US 5,638,367) describes element 655 as a byte rotation circuit and such circuit is DOWNSTREAM of element 660 and register 665.

The Examiner has never responded to Applicant's position that element 600 does not:

shift the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently gathered one of the packets and the number of bytes in a prior gathered one of the packets.

As pointed out in claim 2, the system includes:

a shifter for shifting the bytes stored in the sampling register, such bytes being shifted as a function of the offset of the currently distributed one of the packets and the number of bytes in a prior distributed one of the packets;

Thus, the shifter in claim 2 is, for the reasons set forth above, not element 600 in Gaytan et al.

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

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Date

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